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Representing Weighted Binary Codes using FPGA

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ABSTRACT

Nowadays machines are playing major role in any development. We need a language or code to communicate with machine. These language or codes must be machine readable and acceptable. Several weighted binary codes have been developed to simplify the communication process between man and machine. In this paper, some of weighted binary codes such as 5421, 5211, 2421 and 4221 are represented by using Artix7 series Field Programmable Gate Array (FPGA) board. Very High Speed Hardware Description Language (VHDL) language is used to design a system which represents these weighted binary codes on FPGA board. Two FPGA switches are used to select weighted binary codes. Four bits inputs of each weighted binary codes are passed using four FPGA switches. Four bits output of each weighted binary codes are represented by using seven segment display and four LEDs of FPGA Board. Xilinx Vivado2015.2 tool is used to do the synthesis and simulation of the proposed system.

Keywords: *FPGA, VHDL, Seven segment display, Switches.*

1. Introduction

In digital computers, binary number system is most widely used but in case of communication between man and machine decimal number system are more conventionally used [1]. From the beginning only decimal based computer arithmetic are used for implementing most of the applications [2]. Most of numerical data generated by human beings are decimal numbers, so to simplify communication between man and machine.

Several numeric codes have been developed to represent decimal numbers in the form of BCD codes. BCD codes are two types, weighted and non-weighted codes. Weighted codes follow position-weighting principle. In position weighting principle, each number has a specific weight. There are several binary weighted codes such as 5211, 8421, 2421, 5421, 4221 have been developed. These codes are either positively-weighted or negatively-weighted. Weights assigned to the binary digits are positive in case of positively-weighted codes, where as in case of negatively- weighted codes some of digits have negative weight.

Several researchers have been working on implementing these binary codes. P.Praveena and S.Sathiya designed and implemented 8421 code to unit distance using reversible logic gates [3]. This system was designed using Xilinx software and implementation was done onSparten3 FPGA board. PMOS based binary to gray code conversion circuit was developed by Sowmya Bhat, Avinash N.J, Kusuma Prabhu and Rajashree Nambiar in 2016 [4]. Mentor Graphics tool was used to design and simulate this code converter circuit.

E.Rajalakshmi, A.Jossie Pushpa, and T.P.Deepikajee developed VLSI based binary to Gray conversion circuit using synchronous, asynchronous and asynchronous pipeline register (APR) circuits [5]. P.Sai Lalitha Durgamba and K.Chaitanya [6] designed and implemented a code converter circuits for high speed multiplier applications using cadence technology. Achsa Benjamin, Shreya Suman and Pratima Manhas [7] designed and implemented 4-bit binary-to-gray code converter, 4 bit binary-to-gray, 4-bit BCD-to-excess 3 and 4-bit gray-to-binary code

Converters circuits using Xilinx ISE software. In this paper, a system is developed to represent weighted binary codes such as 2421, 5211, 4221 and 5421on FPGA board. Detail Discussion of this proposed system is discussed in the below sections.

2. Different Types of Weighted Binary Codes

2.1. 5421 Code

In 5421 code, binary weights carry 5,4,2,1 from left to right. Truth Table for 4 bit binary input to 4 bit 5421 code as an output is shown in Table 1. In this Table, 4 bits output for 5421 code is shown in hexadecimal system also. Here A, B, C and D represents four bits binary inputs and X, Y, Z and W represents four bits 5421 code.

Table 1. Truth Table for Binary to 5421 code Conversion

A	B	C	D	X	Y	Z	W	5421 in Hexadecimal
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	3
0	1	0	0	0	1	0	0	4
0	1	0	1	0	1	0	1	5
0	1	1	0	0	1	1	0	6
0	1	1	1	0	1	1	1	7
1	0	0	0	1	0	1	1	8
1	0	0	1	1	1	0	0	9
1	0	1	0	1	1	0	1	a
1	0	1	1	1	1	1	0	b
1	1	0	0	1	1	1	1	c
1	1	0	1	X	X	X	X	X
1	1	1	0	X	X	X	X	X
1	1	1	1	X	X	X	X	X

2.2. 5211 Code

In 5211 code, binary weights carry 5,2,1,1 from left to right. Truth Table for 4 bit binary input to 4 bit 5211 code as an output is shown in Table 2. In this Table, 4 bits output for 5211 code is shown in hexadecimal system also. Here A, B, C and D represents four bits binary inputs and X, Y, Z and W represents four bits 5211 code.

Table 2. Truth Table for Binary to 5211 code Conversion

A	B	C	D	X	Y	Z	W	5211 in Hexadecimal
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	2
0	0	1	1	0	1	0	1	3
0	1	0	0	0	1	1	1	4
0	1	0	1	1	0	0	0	5
0	1	1	0	1	0	1	0	6
0	1	1	1	1	1	0	0	7
1	0	0	0	1	1	1	0	8
1	0	0	1	1	1	1	1	9
1	0	1	0	X	X	X	X	X
1	0	1	1	X	X	X	X	X
1	1	0	0	X	X	X	X	X
1	1	0	1	X	X	X	X	X
1	1	1	0	X	X	X	X	X
1	1	1	1	X	X	X	X	X

2.3. 2421 Code

In 2421 code, binary weights carry 2,4,2,1 from left to right. Truth Table for 4 bit binary input to 4 bit 2421 code as an output is shown in Table 3. In this Table, 4 bits output for 2421 code is shown in hexadecimal system also. Here A, B, C and D represents four bits binary inputs and X, Y, Z and W represents four bits 2421 code.

Table 3. Truth Table for Binary to 2421 code Conversion

A	B	C	D	W	X	Y	Z	2421 in Hexadecimal
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	3

0	1	0	0	0	1	0	0	4
0	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	6
0	1	1	1	1	1	0	1	7
1	0	0	0	1	1	1	0	8
1	0	0	1	1	1	1	1	9
1	0	1	0	X	X	X	X	X
1	0	1	1	X	X	X	X	X
1	1	0	0	X	X	X	X	X
1	1	0	1	X	X	X	X	X
1	1	1	0	X	X	X	X	X
1	1	1	1	X	X	X	X	X

2.4. 4221 Code

In 4221 code, binary weights carry 4,2,2,1 from left to right. Truth Table for 4bit binary input to 4 bit 4221 code as an output is shown in Table 4. In this Table, 4 bits output for 4221 code is shown in hexadecimal system also. Here A, B, C and D represents four bits binary inputs and X, Y, Z and W represents four bits 4221 code.

Table 4. Truth Table for Binary to 4221 code Conversion

A	**B**	**C**	**D**	**W**	**X**	**Y**	**Z**	**4221 in Hexadecimal**
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	3
0	1	0	0	0	1	1	0	4
0	1	0	1	0	1	1	1	5
0	1	1	0	1	0	1	0	6
0	1	1	1	1	0	1	1	7
1	0	0	0	1	1	1	0	8
1	0	0	1	1	1	1	1	9

1	0	1	0	X	X	X	X	X
1	0	1	1	X	X	X	X	X
1	1	0	0	X	X	X	X	X
1	1	0	1	X	X	X	X	X
1	1	1	0	X	X	X	X	X
1	1	1	1	X	X	X	X	X

3. Representation of Weighted Binary Codes Using FPGA

In this paper, four binary weighted codes named as 5421, 5211, 2421, and 4221 are represented using artix7 series FPGA board. For testing, four bits inputs are passed using four FPGA switches named as Pin W14, Pin_V15, Pin_W15, and Pin_W17. At a time one of weighted binary codes are selected by two FPGA switches named as Pin_ V16 and Pin _W16. If Pin_ V16 and Pin _W16 value is "00" then 5421 code is selected. If Pin_ V16 and Pin _W16 value is "01" then 4221 code is selected. If Pin_ V16 and Pin _W16 value is "10" then 2421 code is selected. If Pin_ V16 and Pin _W16 value is "11" then 5211 code is selected. Output for each binary weighted code is displayed using four FPGA LEDs. For better understanding outputs are displayed in hexadecimal format by using seven segment displays. FPGA pin description for implementing this system is shown in Table 5. Seven segment display codes for displaying the outputs in hexadecimal format are shown in Table 6.

Table 5. FPGA pin Description for the proposed weighted binary code System

Input (4 bit) **FPGA Switches** **Pin_W14Pin_V15Pin_W15Pin_W17**	**Selection line So** **FPGA Switches** **Pin_V16**	**Selection line S1** **FPGA Switches** **Pin _W16**	**Seven Segment Display Output (FPGAPIN _U2)**
5421 code	0	0	Output for 5421 code in Hexadecimal form
4221 code	0	1	Output for 4221 code in Hexadecimal form
2421 code	1	0	Output for 2421 code in Hexadecimal form
5211 code	1	1	Output for 5211 code in Hexadecimal form

Table 6. Seven Segment Display Code Common anode type

Input(3)	Input(2)	Input(1)	Input(0)	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0	0	0	0
0	1	0	0	1	0	1	1	0	0	0
1	1	0	1	0	0	1	0	0	1	0
0	1	1	0	0	0	0	0	0	1	0
0	1	1	1	0	1	1	1	0	0	0
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	0	1	1	1	0	0	0	0	1	0
1	1	0	0	0	0	0	0	1	1	1
1	1	0	1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	0	0	0	1	1	1	0

4. Experimental Results for the Implemented Binary Weighted Code System

The proposed binary code system is designed using VHDL. Artix7 FPGA board (xc7a35cpg236-1) [8] is used to implement this system. Vivado2015.2 tool is used to do synthesis and simulation. RTL diagram for the implemented weighted binary system is shown in Fig.1.

Simulation waveform for the proposed weighted binary system is shown in Fig.2. Synthesis result for this system is shown in Table 7. Representation of 5421 code for displaying hexadecimal number ‘a’ is shown in Fig.3. Representation of 5421 code for displaying hexadecimal number ‘9’ is shown in Fig.4. Representation of 4221 code for displaying hexadecimal number ‘8’ is shown in Fig.5.

Representation of 4221 code for displaying hexadecimal number ‘9’ is shown in Fig.6. Representation of 2421 code for displaying hexadecimal number ‘6’ is shown in Fig.7.

Representation of 2421 code for displaying hexadecimal number ‘9’ is shown in Fig.8. Representation of 5211 code for displaying hexadecimal number ‘2’ is shown in Fig.9. Representation of 5211 code for displaying hexadecimal number ‘3’ is shown in Fig.10.

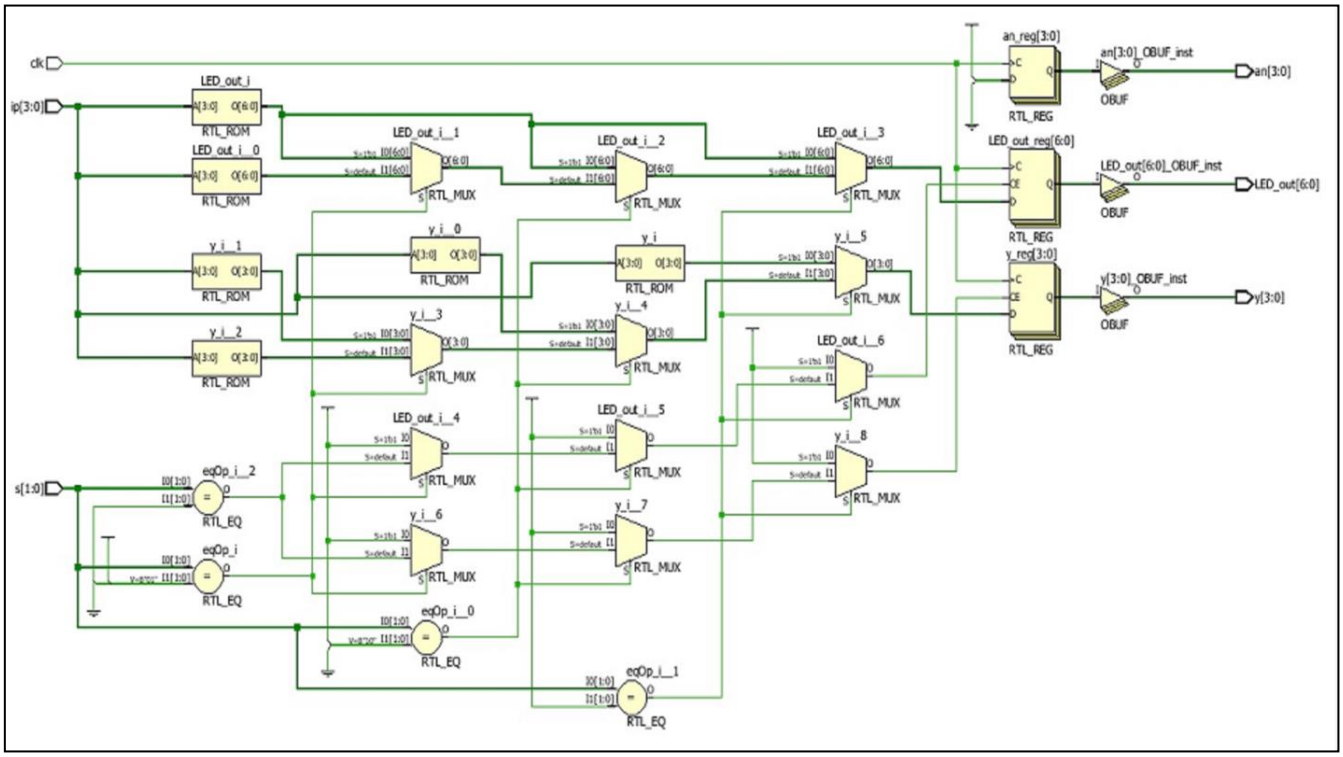

Fig.1. RTL Diagram For weighted binary system

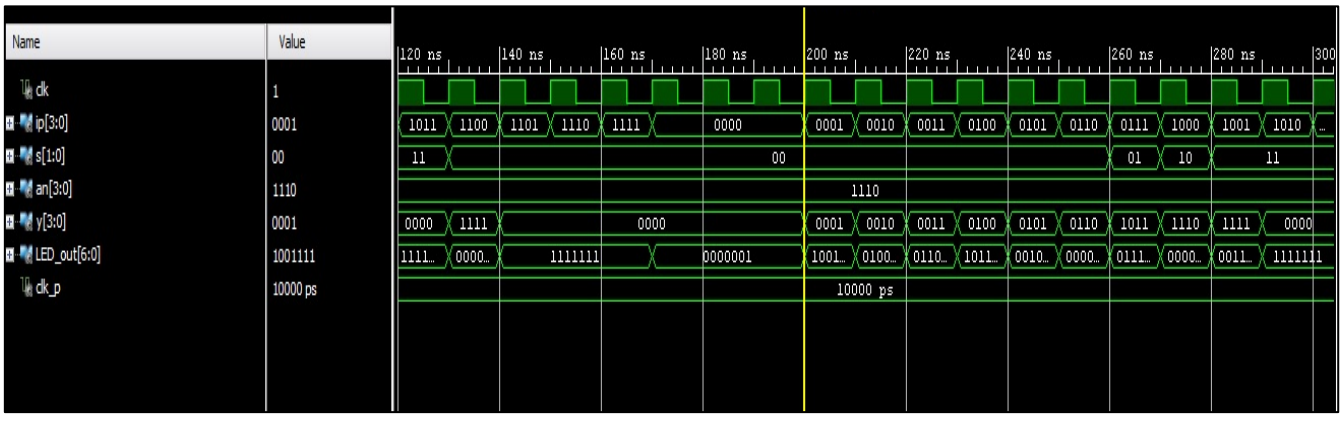

Fig.2. Simulation waveform for the weighted binary system

Table 7. Synthesis Results for Weighted Binary Code System

FPGA Board	Area (LUT)	Speed (ns)	Power (watt)
Artix7	11	6.519	0.087

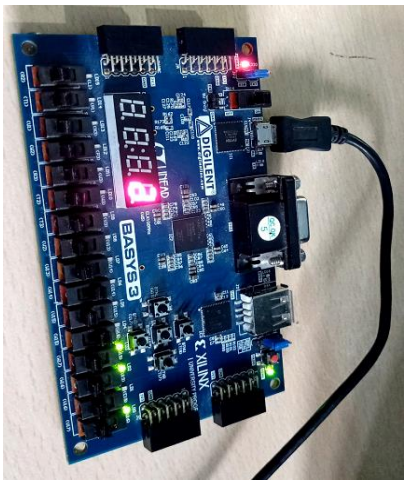

Fig.3. Representation of 5421 code for displaying hexadecimal number ‘a’

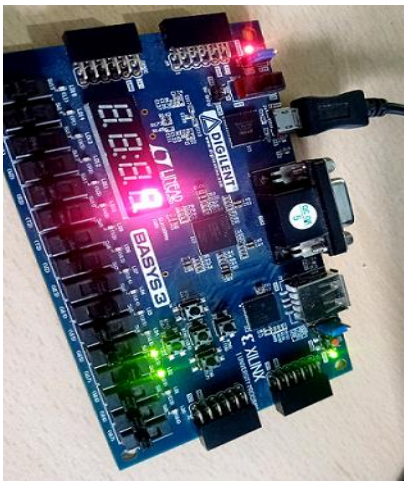

Fig.4. Representation of 5421 code for displaying hexadecimal number ‘9’

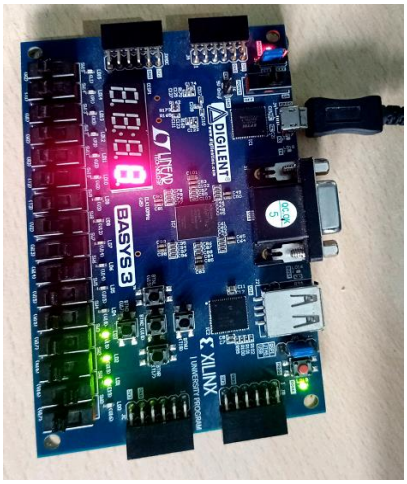

Fig.5. Representation of 4221 code for displaying hexadecimal number ‘8’

Fig.6. Representation of 4221 code for displaying hexadecimal number ‘9’

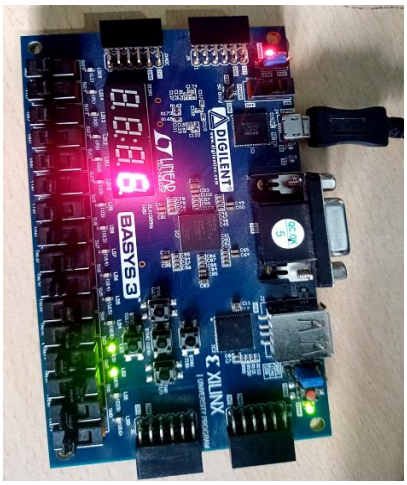

Fig.7. Representation of 2421 code for displaying hexadecimal number ‘6’

Fig.8. Representation of 2421 code for displaying hexadecimal number ‘9’

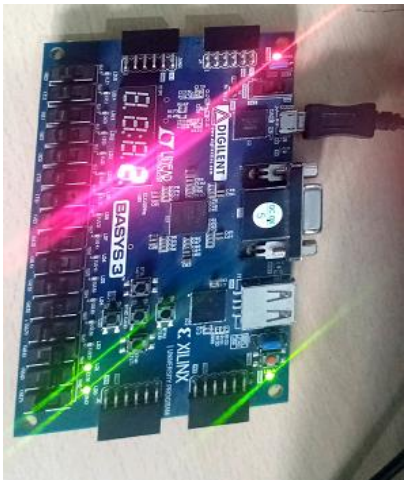

Fig.9. Representation of 5211 code for displaying hexadecimal number '2'

Fig.10. Representation of 5211 code for displaying hexadecimal number '3'

5. Conclusion

In this paper, to represent weighted binary numbers a system is developed using VHDL. Weighted binary codes such as 2421, 4221, 5421 and 5211 are represented using FPGA board. Proposed system is tested for all combinations of four bits inputs. Simulation waveform and FPGA outputs are displayed using seven segment display and four LEDs of FPGA board. 11 LUTs are consumed by the proposed system. Data path delay of this system is 6.519 ns. Total on chip power consumption of this implemented system is 0.087w. Proposed system can be used for implementing communication between man and machine.

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Competing Interests Statement

The authors declare no competing financial, professional and personal interests.

Consent for publication

Authors declare that they consented for the publication of this research work.

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